REMARKS/ARGUMENTS

Favorable reconsideration of this application in view of the above amendments and in light of the following discussion is respectfully requested.

Claims 1-12 and 15-21 are pending. Claims 1 and 3 are amended. No new matter is introduced.

In the outstanding Office Action, Claims 1-3, 5, 7, 8, 11, and 15-19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Byers (U.S. Patent No. 6,906,407) in view of Nagesh (U.S. Patent No. 5,585,671).

Claims 4, 6, 9, 10, and 12 were objected to as dependent upon a rejected base claim, but indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and Claims 20 and 21 were indicated as allowed. The indication of allowed and allowable subject matter is gratefully acknowledged. For the reasons discussed below, all of the claims are believed to be in condition for allowance.

Applicants acknowledge with appreciation the courtesy of Examiner Dinh to interview this case with Applicants' representatives on December 20, 2007, during which time the issues in the outstanding Office Action were discussed as substantially summarized hereinafter and also on the Interview Summary.

During the personal interview, the features of the packaging structure recited in Claims 1 and 3 were discussed. Following from this discussion, Claim 1 is amended to clarify that the package structure is mounted on the interposer and has a *through-opening to receive* the LSI to allow the dissipation member to be located above the surface of the LSI. Also following from this discussion, Claim 3 is amended to clarify that the package structure is mounted on the interposer and has a *through-opening to receive* the LSI to allow the heat dissipation member to be located on the surface of the LSI.

Neither Byers nor Nagesh, either alone or in combination, disclose or suggest the package structure recited in Claims 1 or 3.

Figure 2 of Byers illustrates a gate array assembly 100. The gate array assembly 100 includes a bottom integrated circuit 102 and a top integrated circuit 104.[1] The bottom integrated circuit 102 and top integrated circuit 104 are electrically and mechanically coupled together.[2] Bottom integrated circuit 102 includes a cavity-up ball grid array package 107 that is electromechanically coupled to printed circuit board 106.[3] An integrated circuit (IC) die 10 is coupled to package 107 in a flip chip style via solder balls 112.[4]

However, as can be seen in Figure 2 of Byers, none of the elements of the gate array assembly 100 include a *through-opening* to receive an LSI to allow a heat dissipation member to be either located above or on the surface of the LSI.

Nagesh fails to cure the deficiencies in Byers. Figure 1 of Nagesh illustrates a flip chip IC package 10 that includes an integrated circuit chip or die 12 mounted on a substrate 14.[5] Solder bumps form interconnects between circuitry formed on an inverted interconnect side of the chip 12 and the upper side of the substrate 14.[6] The substrate 14 includes electrical connections 26 that coupling the package to a printed circuit board 28.[7] A heat sink frame 30 is mounted on the printed circuit board 28 to receive a heat sink 32.[8] A heat sink-lid interface layer 34 and heat sink support structure 36 provide a thermal connection between the lid 20 and the heat sink 32.[9] However, Nagesh fails to disclose or suggest any structure that could reasonably be interpreted as the claimed package.

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[1] See Byers, at col. 3, lines 5-7.
[2] See Byers, at col. 3, lines 7-10.
[3] See Byers, at col. 3, lines 43-49.
[4] See Byers, at col. 4, lines 1-2.
[5] See Nagesh,, at col. 4, lines 14-17.
[6] See Nagesh,, at col. 4, lines 17-20.
[7] See Nagesh, at col. 4, lines 34-37.
[8] See Nagesh, at col. 4, lines 37-39.
[9] See Nagesh, at col. 4, lines 39-42.

Claims 1 and 3 each recite an interface module that includes signal transmission lines configured to transmit signals to outside and to receive the signals from outside, second coupling parts electrically connected to the signal transmission lines, and a package structure *configured to hold the signal transmission lines and the second coupling parts*. Nagesh fails to disclose or suggest a structure that is configured to hold signal transmission lines or the claimed second coupling parts, much less such a structure that also includes a *through-opening* to receive an LSI to allow a heat dissipation member to be either located above or on the surface of the LSI.

Accordingly, even the combined teachings of Byers and Nagesh fail to disclose or suggest the features recited in Claims 1 or 3. It is submitted that Claims 1 and 3, and the claims depending therefrom, are in condition for allowance.

For the reasons discussed above, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. Therefore a Notice of Allowance for Claims 1-12 and 15-21 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better condition for allowance, the Examiner is encouraged to contact Applicants' undersigned representative at the below-listed telephone number.

Respectfully submitted,

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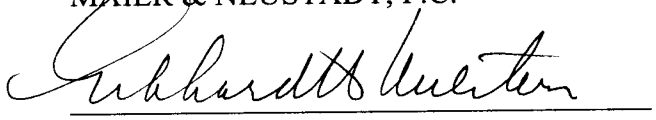

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